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(54) **HIGH VOLTAGE METAL-OXIDE-SEMICONDUCTOR TRANSISTOR DEVICE**

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H01L 29/08 (2006.01)

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CPC ***H01L 29/78*** (2013.01); ***H01L 29/063*** (2013.01); ***H01L 29/0653*** (2013.01); ***H01L 29/0878*** (2013.01); ***H01L 29/7816*** (2013.01); *H01L 29/0692* (2013.01)

(58) **Field of Classification Search**

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See application file for complete search history.

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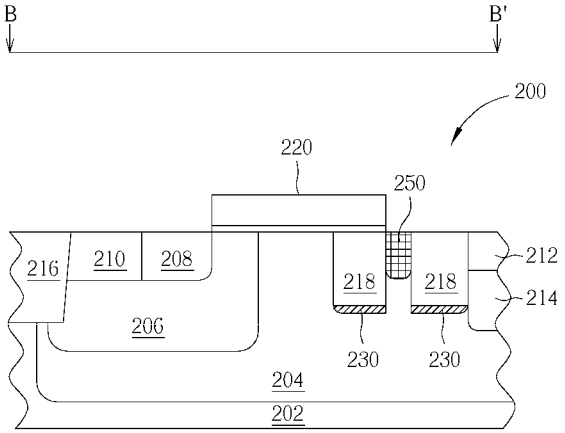
(57) **ABSTRACT**

A HV MOS transistor device is provided. The HV MOS transistor device includes a substrate comprising at least an insulating region formed thereon, a gate positioned on the substrate and covering a portion of the insulating region, a drain region and a source region formed at respective sides of the gate in the substrate, and a first implant region formed under the insulating region. The substrate comprises a first conductivity type, the drain, the source, and the first implant region comprise a second conductivity type, and the first conductivity type and the second conductivity type are complementary to each other.

15 Claims, 5 Drawing Sheets



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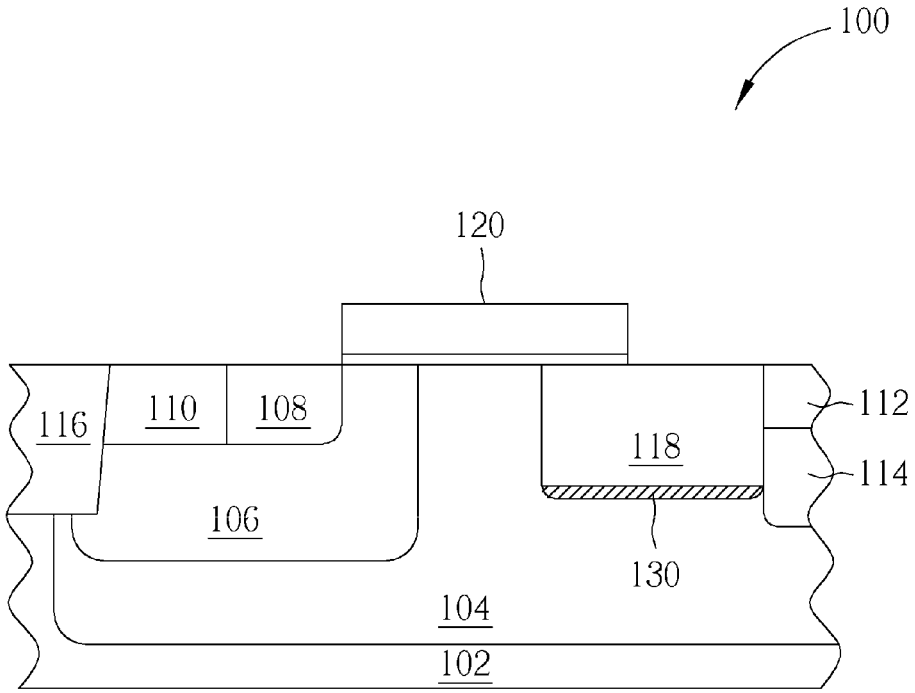
100
120
116
110
108
112
118
114
106
130
104
102

FIG. 1

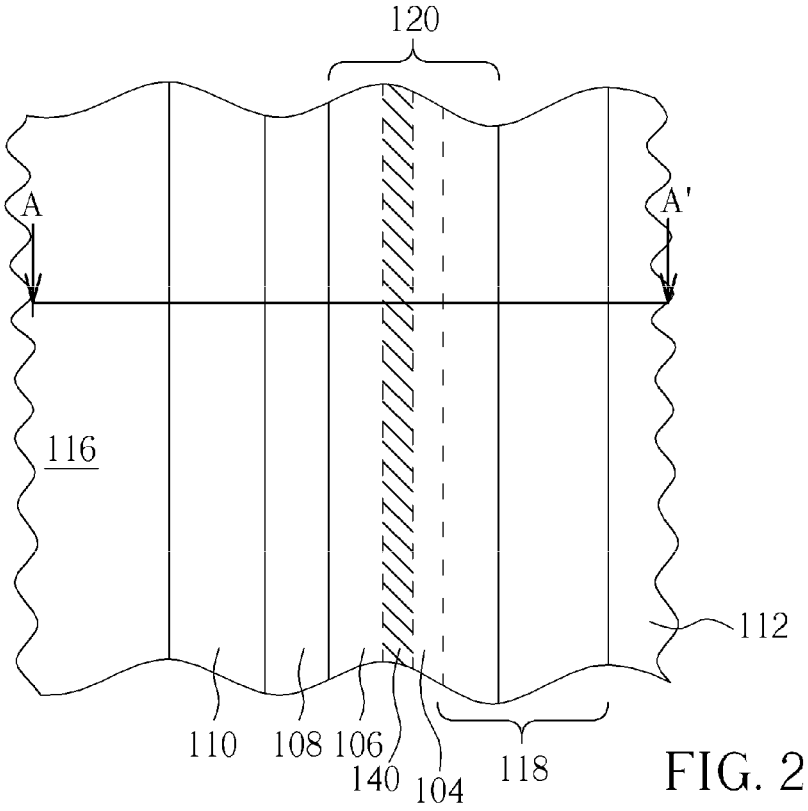
120
A
A'
116
112
110
108
106
140
104
118

FIG. 2

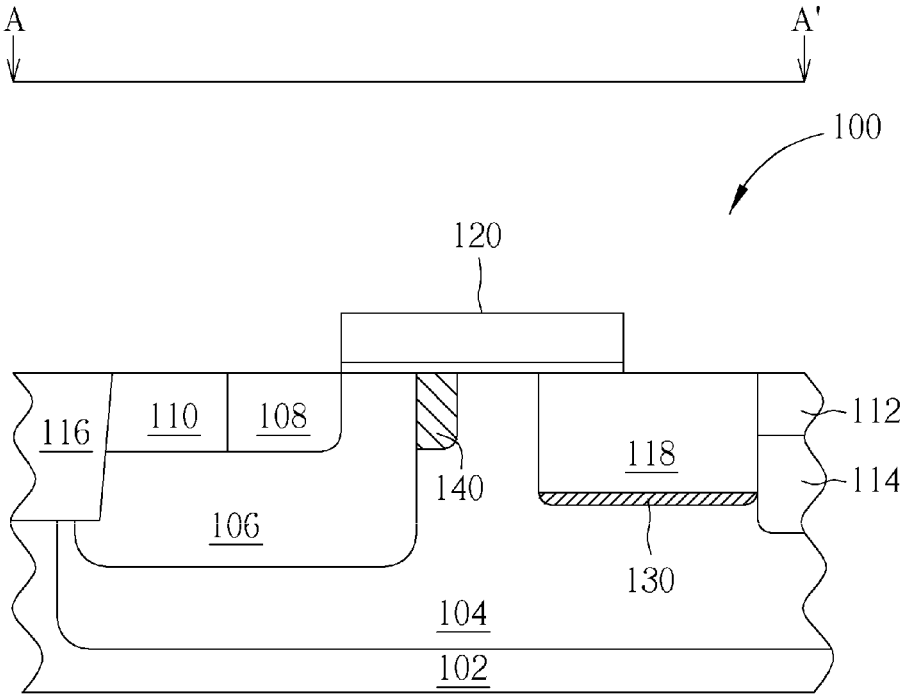
A
A'
100
120
116
110
108
140
118
112
114
106
130
104
102

FIG. 3

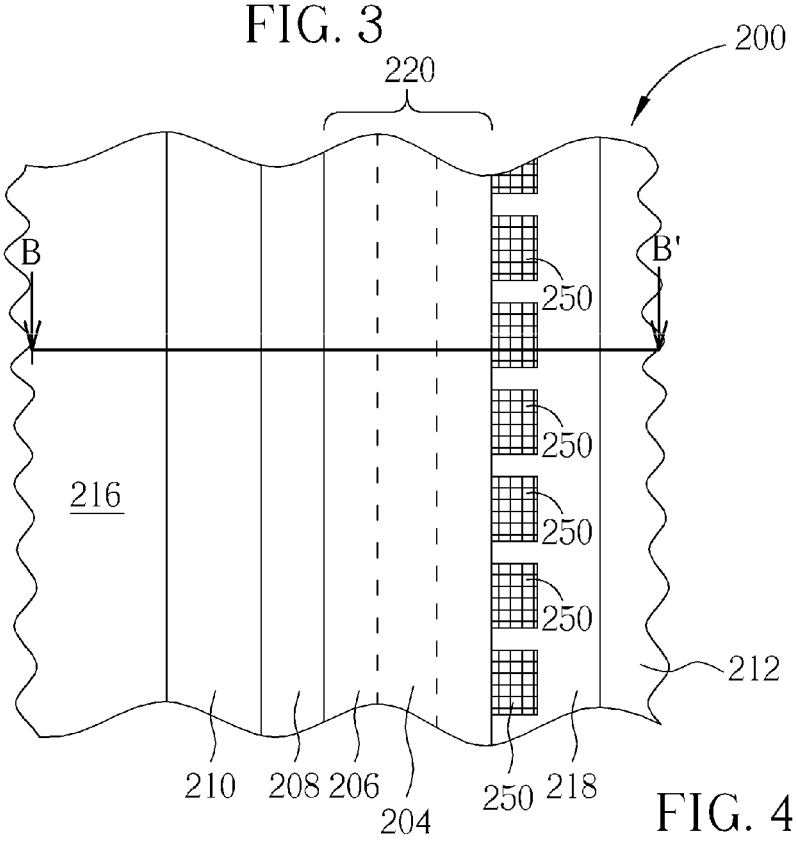
200
220
B
B'
250
250
250
250
216
212
210
208
206
204
250
218

FIG. 4

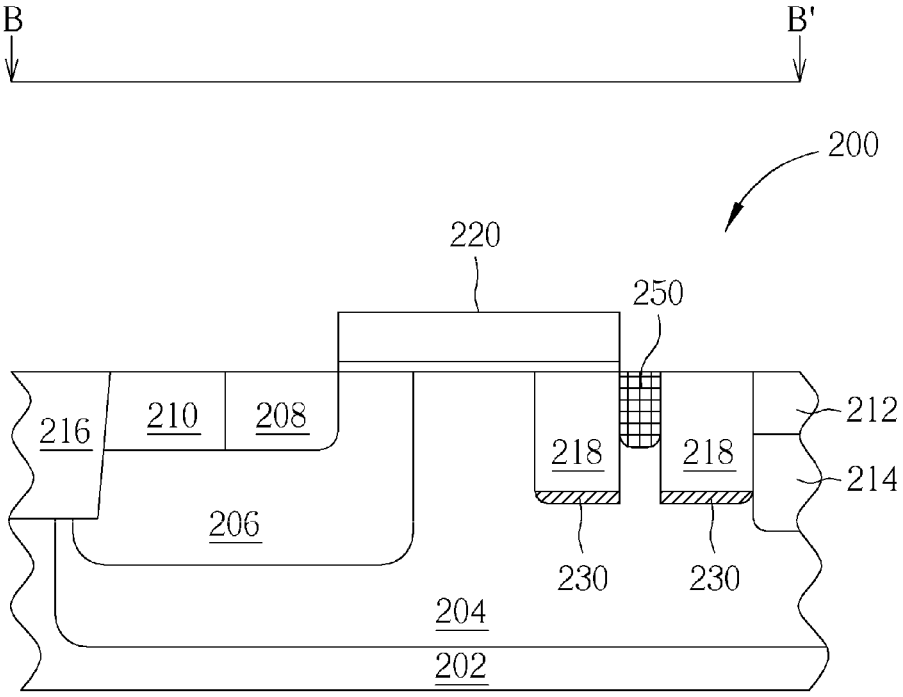
B
B'
200
220
250
216
210
208
218
218
212
214
206
230
230
204
202

FIG. 5

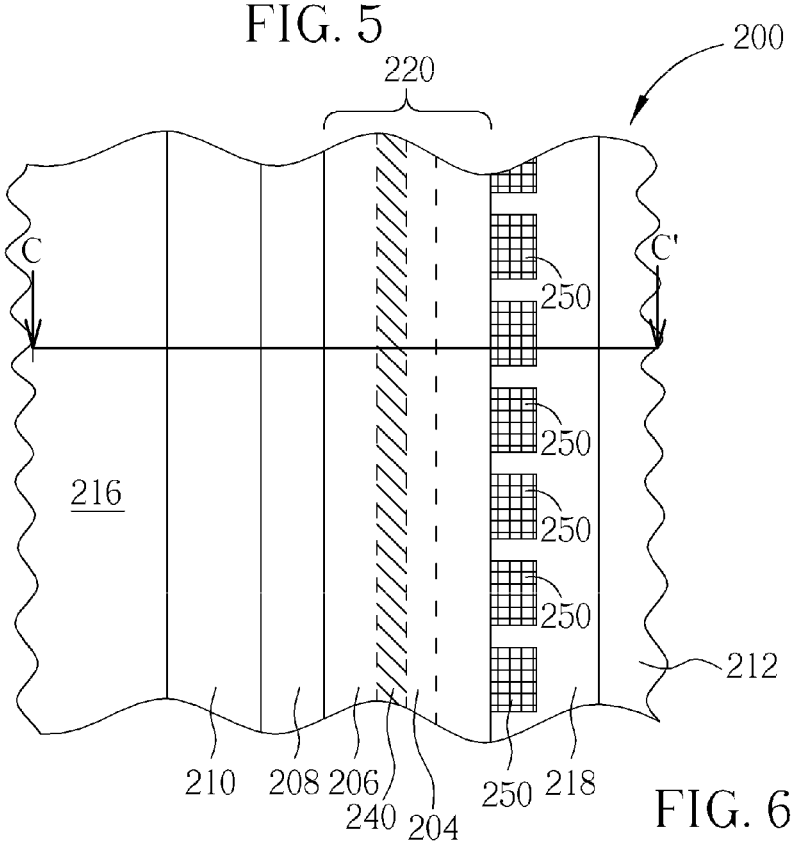
200
220
C
C'
250
250
250
250
216
212
210
208
206
240
204
250
218

FIG. 6

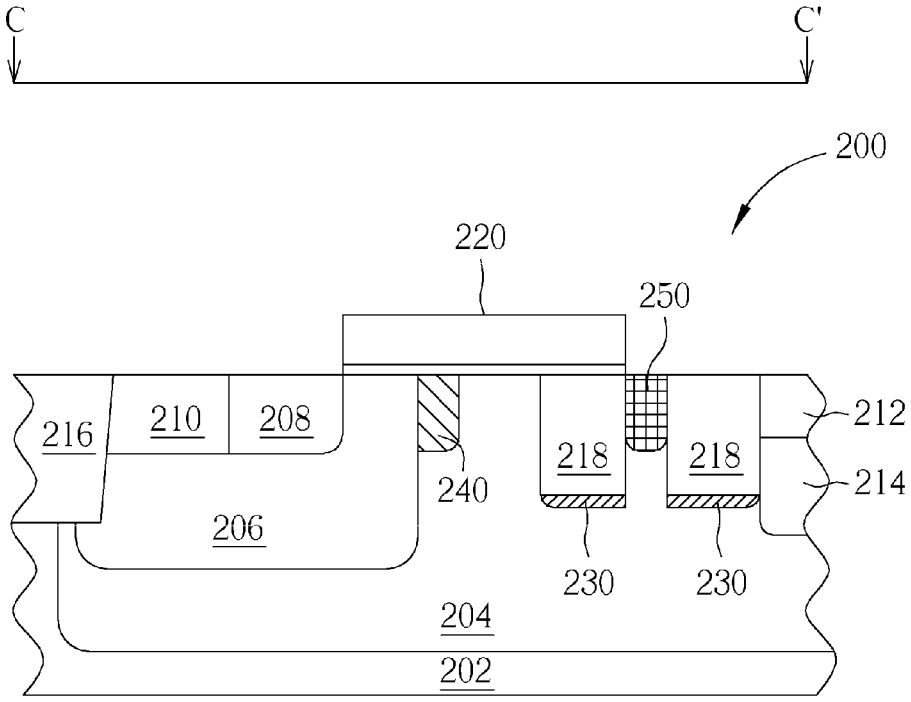
C
C'
200
220
250
216
210
208
240
218
218
212
214
206
230
230
204
202

FIG. 7

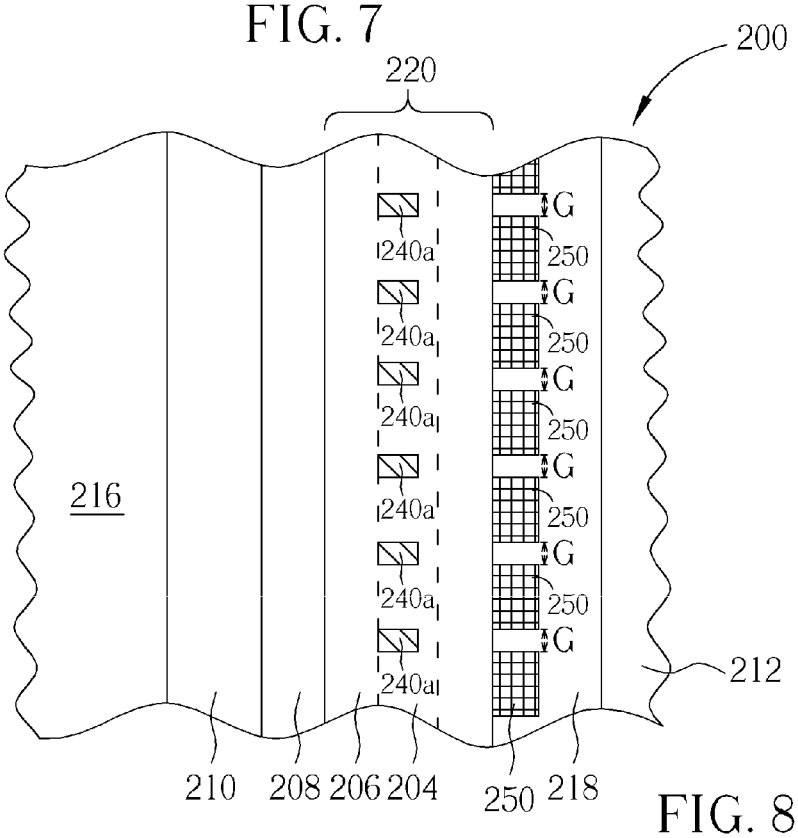
200
220
G
240a
250
216
212
210
208
206
204
250
218

FIG. 8

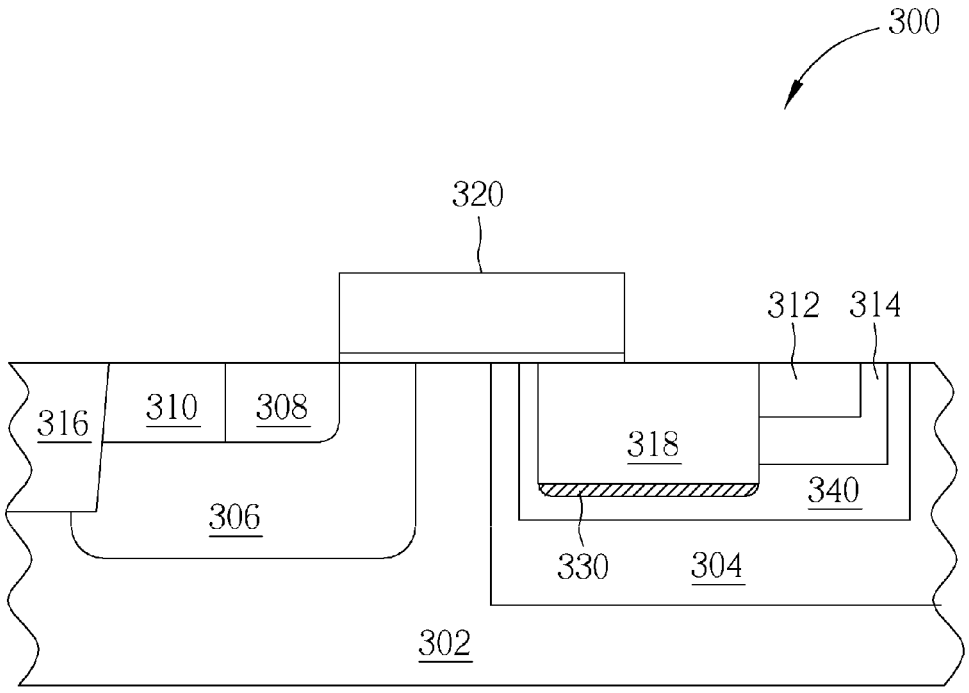

FIG. 9

HIGH VOLTAGE METAL-OXIDE-SEMICONDUCTOR TRANSISTOR DEVICE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The invention relates to a high voltage metal-oxide-semiconductor (herein after abbreviated as HV MOS) transistor device, and more particularly, to a high voltage lateral double-diffused metal-oxide-semiconductor (HV-LDMOS) transistor device.

2. Description of the Prior Art

Double-diffused MOS (DMOS) transistor devices have drawn much attention in power devices having high voltage capability. The conventional DMOS transistor devices are categorized into vertical double-diffused MOS (VDMOS) transistor device and lateral double-diffused MOS (LDMOS) transistor device. Having advantage of higher operational bandwidth, higher operational efficiency, and convenience to be integrated with other integrated circuit due to its planar structure, LDMOS transistor devices are prevalently used in high operational voltage environment such as CPU power supply, power management system, AC/DC converter, and high-power or high frequency (HF) band power amplifier. The essential feature of LDMOS transistor device is a lateral-diffused drift region with low dopant concentration and large area. The drift region is used to alleviate the high voltage between the drain and the source, therefore the LDMOS transistor device can have higher breakdown voltage. The dope concentration and length of the lateral-diffused drift region affects the breakdown voltage (BVD) and the ON-resistance (hereinafter abbreviated as R_{ON}) of the HV-LDMOS transistor device.

It is well-known that characteristics of low R_{ON} and high breakdown voltage are always required to the HV MOS transistor device. However, breakdown voltage and R_{ON} are conflicting parameters with a trade-off relationship. Therefore, a HV LDMOS transistor device that is able to realize high breakdown voltage and low R_{ON} is still in need.

SUMMARY OF THE INVENTION

According to the claimed invention, a HV MOS transistor device is provided. The HV MOS transistor device includes a substrate having at least an insulating region formed thereon, a gate positioned on the substrate and covering a portion of the insulating region, a drain region and a source region having a first conductivity type formed at respective sides of the gate in the substrate, and a first implant region having the first conductivity type formed under the insulating region.

According to the HV MOS transistor device provided by the present invention, R_{ON} of the HV MOS transistor is effectively reduced due to the first implant region formed under the insulating region. Therefore the R_{ON}/BVD ratio is desirably lowered.

These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a cross-sectional view of a HV MOS transistor device provided by a first preferred embodiment of the present invention.

FIG. **2** is a schematic drawing of a portion of a layout pattern of a HV MOS transistor device provided by a second preferred embodiment of the present invention.

FIG. **3** is a cross-sectional view of the HV MOS transistor device taken along a line A-A' of FIG. **2**.

FIG. **4** is a schematic drawing of a portion of a layout pattern of a HV MOS transistor device provided by a third preferred embodiment of the present invention.

FIG. **5** is a cross-sectional view of the HV MOS transistor device taken along a line B-B' of FIG. **4**.

FIG. **6** is a schematic drawing of a portion of a layout pattern of a HV MOS transistor device provided by a fourth preferred embodiment of the present invention.

FIG. **7** is a cross-sectional view of the HV MOS transistor device taken along a line C-C' of FIG. **6**.

FIG. **8** is a schematic drawing of a portion of a layout pattern of a HV MOS transistor device provided by a modification to the fourth preferred embodiment.

FIG. **9** is a cross-sectional view of a HV MOS transistor device provided by a fifth preferred embodiment of the present invention.

DETAILED DESCRIPTION

Please refer to FIG. **1**, which is a cross-sectional view of a HV MOS transistor device provided by a first preferred embodiment of the present invention. As shown in FIG. **1**, a HV MOS transistor device **100** provided by the preferred embodiment is positioned on a substrate **102**, such as a silicon substrate. The substrate **102** further includes a deep well region **104** formed therein. The substrate **102** includes a first conductivity type and the deep well region **104** includes a second conductivity type. The second conductivity type and the first conductivity type are complementary to each other. In the preferred embodiment, the first conductivity type is p-type and thus the second conductivity type is n-type. The HV MOS transistor device **100** further includes a gate **120** positioned on the substrate **102**. A body region **106** is formed in the deep well region **104**. The body region **106** includes the first conductivity type and thus is a p-body region **106**. A source region **108** and a drain region **112** are formed in the substrate **102** at respective sides of the gate **120**. Both of the source region **108** and the drain region **112** include the second conductivity type. Accordingly, the preferred embodiment provides an n-source region **108** and an n-drain region **112**. As shown in FIG. **1**, the source region **108** is formed in the p-body region **106**. Furthermore, a p-doped region **110** is formed in the p-body region **106**. The p-doped region **110** is electrically connected to the n-source region **108**. Additionally, an n-well **114** is formed in the deep well region **104** at the drain side. As shown in FIG. **1**, the drain region **112** is formed in the n-well **114**. Moreover, a plurality of shallow trench isolations (STIs) **116** for electrically isolating the HV MOS transistor device **100** from other devices and an insulating region **118** are formed in the substrate **102**. The insulating region **118** preferably includes a STI, but not limited to this. The gate **120** covers a portion of the insulating region **118** as shown in FIG. **1**.

Please still refer to FIG. **1**. The HV MOS transistor device **100** provided by the preferred embodiment further includes a first implant region **130** formed under the insulating region **118**. As shown in FIG. **1**, the insulating region **118** covers the first implant region **130** entirely. The first implant region **130** includes the second conductivity type, therefore the first implant region **130** is an n-typed implant region. A dopant concentration of the first implant region **130** is lower than a dopant concentration of the n-well region **114**, and the dopant

concentration of the n-well region **114** is lower than a dopant concentration of the source region **108** and of the drain region **112**.

According to the first preferred embodiment, the n-type first implant region **130** entirely formed under the insulating region **118** effectively reduces R_{ON} of the HV MOS transistor device **100**. Therefore the R_{ON}/BVD ratio is desirably lowered.

Please refer to FIGS. **2-3**, wherein FIG. **2** is a schematic drawing of a portion of a layout pattern of a HV MOS transistor device provided by a second preferred embodiment of the present invention, and FIG. **3** is a cross-sectional view of the HV MOS transistor device taken along a line A-A' of FIG. **2**. It is noteworthy that elements the same in both of the first and second embodiments are designated by the same numerals, and details concerning those elements are omitted in the interest of brevity. As shown in FIGS. **2-3**, the difference between the first and second preferred embodiment is: the HV MOS transistor device **100** provided by the second preferred embodiment further includes a second implant region **140**.

As shown in FIGS. **2-3**, the second implant region **140** is formed in the substrate **102** near the source region **108** and is entirely covered by the gate **120**. More important, the second implant region **140** is spaced apart from the source region **108** by the body region **106** while the second implant region **140** is also spaced apart from the insulating region **118** by the deep well region **104**. According to the preferred embodiment, the second implant region **140** includes a continuous region as shown in FIG. **2**, but not limited to this. A depth of the second implant region **140** is smaller than a depth of the insulating region **118**. The second implant region **140** includes the second conductivity, which means the second implant region **140** is an n-type implant region. A dopant concentration of the second implant region **140** is lower than a dopant concentration of the first implant region **130**, the dopant concentration of the first implant region **130** is lower than a dopant concentration of the source region **108** and the drain region **112**.

According to the HV MOS transistor device **100** provided by the second preferred embodiment, the n-typed first implant region **130** entirely formed under the insulating region **118** effectively reduces R_{ON} of the HV MOS transistor device **100**. More important, R_{ON} is further reduced due to the n-typed second implant region **140** at the source side. Therefore the R_{ON}/BVD ratio of the HV MOS **100** provided by the second preferred embodiment is further lowered. Additionally, an additional n-drift region can further enhance the performance of the HV MOS transistor device **100**.

Please refer to FIGS. **4-5**, wherein FIG. **4** is a schematic drawing of a portion of a layout pattern of a HV MOS transistor device provided by a third preferred embodiment of the present invention, and FIG. **5** is a cross-sectional view of the HV MOS transistor device taken along line B-B' of FIG. **4**. As shown in FIGS. **4-5**, a HV MOS transistor device **200** provided by the preferred embodiment is positioned on a substrate **202**. The substrate **202** further includes a deep well region **204** formed therein. Please note that the elements the same in the first, second, and third preferred embodiments include the same conductivity types, therefore those details are omitted for simplicity. The HV MOS transistor device **200** further includes a gate **220** positioned on the substrate **202**. A body region **206** is formed in the deep well region **204**. A source region **208** and a drain region **212** are formed in the substrate **202** at respective sides of the gate **220**. As shown in FIG. **5**, the source region **208** is formed in the p-body region **206**. Furthermore, a p-doped region **210** electrically connected to the n-source region **208** is formed in the p-body region **206**. Additionally, an n-well **214** is formed in the deep well region **204** at the drain side. As shown in FIG. **5**, the drain region **212** is formed in the n-well **214**. Moreover, a plurality of STIs **216** for electrically isolating the HV MOS transistor device **200** from other devices and an insulating region **218** are formed in the substrate **202**. The insulating region **218** preferably includes a STI, but not limited to this. The gate **220** covers a portion of the insulating region **218** as shown in FIGS. **4-5**.

Please refer to FIGS. **4-5** again. The HV MOS transistor device **200** provided by the third preferred embodiment further includes a plurality of diffusion islands **250** surrounded by the insulating region **218**, and the diffusion islands **250** are spaced apart from each other by the insulating region **218**. Furthermore, a depth of the diffusion islands **250** is smaller than a depth of the insulating region **218**. The diffusion islands **250** include a first conductivity type, which is complementary to the second conductivity type as mentioned above. In other words, the diffusion islands **250** are all p-typed.

Please still refer to FIG. **5**. The HV MOS transistor device **200** provided by the second preferred embodiment still includes a first implant region **230** formed under the insulating region **218**. As shown in FIG. **5**, the insulating region **218** covers the first implant region **230** entirely. The first implant region **230** includes the second conductivity type. A dopant concentration of the first implant region **230** is lower than a dopant concentration of the n-well region **214**, and the dopant concentration of the n-well region **214** is lower than a dopant concentration of the source region **208** and of the drain region **212**.

According to the third preferred embodiment, the n-typed first implant region **230** entirely formed under the insulating region **218** effectively reduces R_{ON} of the HV MOS transistor device **200**. Furthermore, the p-typed diffusion islands **250** surrounded by the insulating region **218** provides a Reduced Surface Field (hereinafter abbreviated as RESURF) effect, therefore the current path of the HV MOS transistor **200** is shorter and the breakdown voltage in the vertical direction is improved. Since R_{ON} is reduced while the breakdown voltage is increased, the R_{ON}/BVD ratio of the HV MOS transistor device **200** provided by the third preferred embodiment is further lowered.

Please refer to FIGS. **6-8**, wherein FIG. **6** is a schematic drawing illustrating a portion of layout pattern of a HV MOS transistor device provided by a fourth preferred embodiment of the present invention, FIG. **7** is a cross-sectional view taken along line C-C' of FIG. **6**, and FIG. **8** is a schematic drawing illustrating a portion of a layout pattern of a HV MOS transistor device provided by a modification to the fourth preferred embodiment. It is noteworthy that elements the same in the third and fourth embodiments are designated by the same numerals, and thus details concerning those elements are omitted in the interest of brevity. As shown in FIGS. **6-7**, the difference between the third and fourth preferred embodiment is: the HV MOS transistor device **200** provided by the second preferred embodiment further includes a second implant region **240**.

As shown in FIGS. **6-8**, the second implant region **240** is formed in the substrate **202** near the source region **208** and is entirely covered by the gate **220**. More important, the second implant region **240** is spaced apart from the source region **208** by the body region **206** while the second implant region **240** is also spaced apart from the insulating region **218** by the deep well region **204**. A depth of the second implant region **240** is smaller than a depth of the insulating region **218**. The second implant region **240** includes the second conductivity, which means the second implant region **240** is an n-type implant region. A dopant concentration of the second implant region

240 is lower than a dopant concentration of the first implant region 230, and the dopant concentration of the first implant region 230.

In order to clearly describe the difference between the fourth preferred embodiment and its modification, FIG. 6 and FIG. 8 should be referred together. As shown in FIG. 6, the second implant region 240 includes a continuous region. However, the second implant region 240 can include a plurality of islanding regions 240*a* as shown in FIG. 8. As mentioned above, the HV MOS transistor 200 provided by the fourth preferred embodiment includes the diffusion islands 250 spaced apart from each other by the insulating region 218. In other words, a gap G is formed in between any two adjacent diffusion islands 250. It is noteworthy that each islanding region 240*a* is formed corresponding to the gap G, respectively according to the modification.

According to the fourth preferred embodiment, the n-typed first implant region 230 entirely formed under the insulating region 218 and the n-typed second implant region 240 formed at the source side effectively reduce R_{ON} of the HV MOS transistor device 200. Simultaneously, the p-typed diffusion islands 250 surrounded by the insulating region 218 provides a RESURF effect, therefore the breakdown voltage of the HV MOS transistor device 200 is improved. Since R_{ON} is reduced while the breakdown voltage is increased, the R_{ON}/BVD ratio of the HV MOS 200 provided by the second preferred embodiment is further lowered.

Please refer to FIG. 9, which is a cross-sectional view of a HV MOS transistor device provided by a fifth preferred embodiment of the present invention. As shown in FIG. 9, a HV MOS transistor device 300 provided by the preferred embodiment is positioned on a substrate 302. The substrate 302 further includes a high voltage well (HV well) region 304 and a body region 306 formed therein, and the HV well region 304 and the body region 306 are spaced apart from each other. The substrate 302, the HV well region 304, and the body region 306 all include a first conductivity type. Furthermore, the HV MOS transistor device 300 of the preferred embodiment includes a drift region 340 formed in the HV well region 304, and a doped region 314 formed in the drift region 340. The drift region 340 and the doped region 314 include a second conductivity type. The second conductivity type and the first conductivity type are complementary to each other. In the preferred embodiment, the first conductivity type is p-type and thus the second conductivity type is n-type.

Pleas still refer to FIG. 9. The HV MOS transistor device 300 further includes a gate 320 positioned on the substrate 302. A source region 308 and a drain region 312 are formed in the substrate 302 at respective sides of the gate 320. Both of the source region 308 and the drain region 312 include the second conductivity type. As shown in FIG. 9, the source region 308 is formed in the p-body region 306. Furthermore, a p-doped region 310 is formed in the p-body region 306. The p-doped region 310 is electrically connected to the n-source region 308. The drain region 312 is formed in doped region 314. As shown in FIG. 9, a plurality of STIs 316 for electrically isolating the HV MOS transistor device 300 from other devices and an insulating region 318 are formed in the substrate 302. The insulating region 318 preferably includes a STI, but not limited to this. As shown in FIG. 9, the insulating region 318 is formed in the drift region 340 and a portion of the insulating region 318 is covered by the gate 320.

Please refer to FIG. 9. The HV MOS transistor device 300 provided by the preferred embodiment further includes a first implant region 330 formed in the drift region 340 and under the insulating region 318. The insulating region 318 covers the first implant region 330 entirely. The first implant region 330 includes the second conductivity type.

According to the first preferred embodiment, the n-typed first implant region 330 entirely formed under the insulating region 318 effectively reduces R_{ON} of the HV MOS transistor device 300. Therefore the R_{ON}/BVD ratio is desirably lowered.

According to the HV MOS transistor device provided by the present invention, R_{ON} of the HV MOS transistor is effectively reduced due to the first implant region formed under the insulating region and the second implant region formed near the source side. Furthermore, the breakdown voltage is improved by the RESURF effect provided by the diffusion islands. Therefore the R_{ON}/BVD ratio is desirably lowered. Furthermore, it should be noted that the HV MOS transistor device provided by the preferred embodiment can employ common source approach or common source approach.

Those skilled in the art will readily observe that numerous modifications and alterations of the device and method may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.

What is claimed is:

1. A high voltage metal-oxide-semiconductor (HV MOS) transistor device comprising:

a substrate comprising at least an insulating region formed thereon, the substrate comprising a first conductivity type;

a gate positioned on the substrate and covering a portion of the insulating region;

a drain region and a source region having a second conductivity type formed at respective sides of the gate in the substrate, and the second conductivity type being complementary to the first conductivity type;

a deep well region formed in the substrate, the deep well region comprising the second conductivity type;

a first implant region having the second conductivity type formed under the insulating region; and

a second implant region formed near the source region, the second implant region is spaced apart from the insulating region by the deep well region, wherein the second implant region comprises a plurality of islanding regions,

wherein the insulating region covers the entire first implant region, and a width of the first implant region is equal to a width of the insulating region.

2. The HV MOS transistor device according to claim **1**, wherein a dopant concentration of the first implant region is lower than a dopant concentration of the source region and the drain region.

3. The HV MOS transistor device according to claim **1**, further comprising a plurality of diffusion islands surrounded by the insulating region, the diffusion islands having the first conductivity type.

4. The HV MOS transistor device according to claim **3**, wherein the diffusion islands are spaced apart from each other by the insulating region.

5. The HV MOS transistor device according to claim **3**, wherein a depth of the diffusion islands is smaller than a depth of the insulating region.

6. The HV MOS transistor device according to claim **1**, wherein the gate covers the second implant region entirely.

7. The HV MOS transistor device according to claim **1**, wherein the second implant region comprises the second conductivity type.

8. The HV MOS transistor device according to claim 1, further comprises a body region having the first conductivity type formed in the substrate.

9. The HV MOS transistor device according to claim 8, wherein the second implant region is spaced apart from the source region by the body region.

10. The HV MOS transistor device according to claim 1, wherein a dopant concentration of the second implant region is lower than a dopant concentration of the first implant region.

11. The HV MOS transistor device according to claim 1, wherein a depth of the second implant region is smaller than a depth of the insulating region.

12. The HV MOS transistor device according to claim 1, further comprising a doped region having the second conductivity type formed in the substrate.

13. The HV MOS transistor device according to claim 12, wherein the drain region, the insulating region, and the first implant region under the insulating region are all formed in the doped region.

14. The HV MOS transistor device according to claim 1, wherein an entire top of the first implant region contacts with a bottom of the insulating region.

15. The HV MOS transistor device according to claim 1, wherein the first implant region is singly formed under the insulating layer in a substrate-thickness direction.

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